WHAT IS CLAIMED IS:

1. An annealing method of annealing an SOI substrate in a reducing atmosphere, comprising the step of:

holding the SOI substrate by a holding portion having a surface formed from silicon and annealing the SOI substrate.

2. The method according to claim 1, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

3. The method according to claim 1, wherein the annealing is executed at a temperature not less than 775℃.

4. The method according to claim 1, wherein the annealing is executed at a temperature not less than 966℃.

5. The method according to claim 1, wherein the annealing is executed at a temperature not less than 993℃.

6. An SOI substrate manufactured using an annealing method of any one of claims 1.

7. The substrate according to claim 6, wherein an HF defect density is not more than 0.05 defects/cm^2.

8. A semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of any one of claims 1; and

forming an active region for a transistor in a

nonporous semiconductor layer of the SOI substrate.

9. A semiconductor device comprising:

an SOI substrate of claim 6; and

an active region for a transistor, which is formed in a nonporous semiconductor layer of the SOI substrate.

10. An annealing method of annealing an SOI substrate in a reducing atmosphere, comprising the step of:

holding the SOI substrate by a holding portion which contains no silicon carbide formed by sintering and has a surface formed from silicon carbide deposited by CVD and annealing the SOI substrate.

11. The method according to claim 10, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

12. The method according to claim 10, wherein the annealing is executed at a temperature not less than 775℃.

13. The method according to claim 10, wherein the annealing is executed at a temperature not less than 966℃.

14. The method according to claim 10, wherein the annealing is executed at a temperature not less than 993℃.

15. An SOI substrate manufactured using an annealing method of any one of claims 10.

16. The substrate according to claim 15, wherein an

HF defect density is not more than 0.05 defects/cm^2.

17. A semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of any one of claims 10; and

forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate.

18. A semiconductor device comprising:

an SOI substrate of claim 15; and

an active region for a transistor, which is formed in a nonporous semiconductor layer of the SOI substrate.